APPLICATION NOTE

Designing an Inverting Buck-boost Converter with MagI³C Power Module WPMDH1302401 / 171032401
(6 - 42 V_{IN} / 3A / 5 - 24 V_{OUT})

ANS007B BY CHRISTOPHER RICHARDSON

1. Introduction

MagI³C Power Modules from Würth Elektronik eiSos are normally used as synchronous buck regulators, capable of stepping down a higher input voltage to a lower output voltage with high efficiency and a compact, low-EMI footprint. The inverting buck-boost is another topology that can be implemented with the MagI³C Power Module family using just a few adjustments. This topology converts a positive input voltage, V_{IN}, into a negative output voltage, $-V_{OUT}$, and the magnitude of $-V_{OUT}$ can be both greater than and less than the magnitude of V_{IN}.

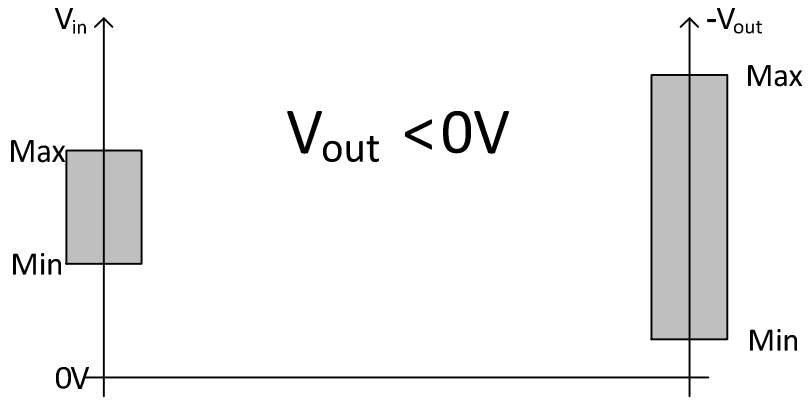

Figure 1: Input and Output voltage range

Input voltage range and the absolute value of the output voltage range can overlap when using an inverting buck-boost regulator. This application note will explain how to select the eternal components for the inverting buck-boost topology and show how the buck topology evaluation boards can be used for buck-boost as well. Figure 2 shows how a inverting buck-boost topology can be derived from a synchronous buck by reassigning the ground and output terminals and modifying the connection of the input capacitor.

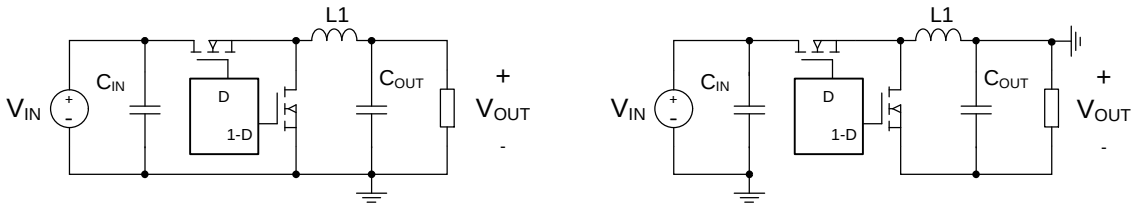

Figure 2: Synchronous buck (left) and synchronous inverting buck-boost (right)

APPLICATION NOTE

Designing an Inverting Buck-boost Converter with MagI³C Power Module WPMDH1302401 / 171032401
(6 - 42 V_{IN} / 3A / 5 - 24 V_{OUT})

Figure 3 shows the basic schematic of a MagI³C Power Module from the VDRM family operating as a synchronous buck on the left, and then the changes needed for an inverting buck-boost on the right. Implementing the circuits of Figures 2 and 3 would not require C_{IN1}. This capacitor is not shown in the block diagram and its benefit will be explained in section 4.7.1.

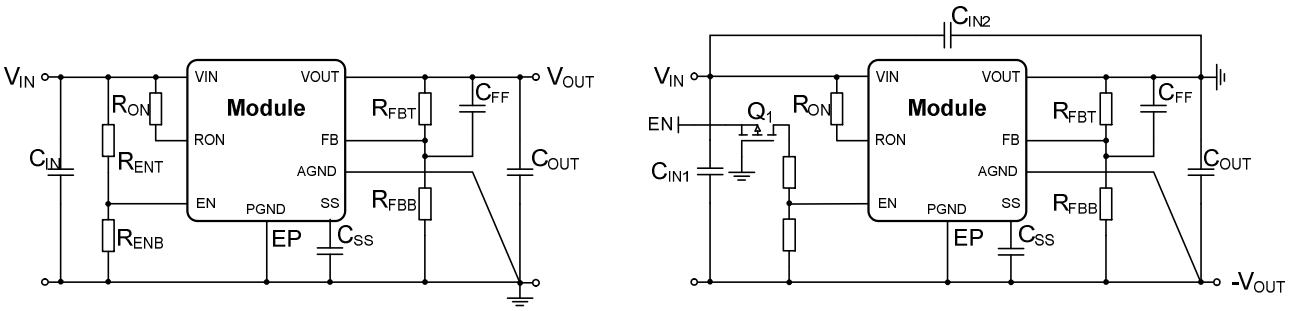

Figure 3: Synchronous buck (left) and inverting buck-boost (right) using VDRM family modules

2. Voltages and Currents in the Synchronous Inverting Buck-boost

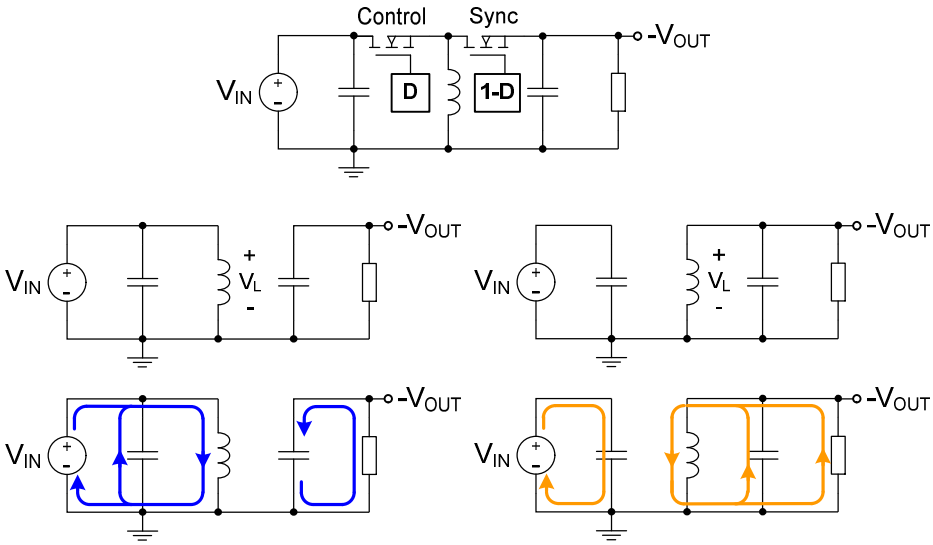

Figure 4: The inverting synchronous buck-boost converter with the control MOSFET on (left) and with the sync MOSFET on (right). Duty cycle, D, is defined in EQ.2 below

Figure 4 shows the two switching states of the synchronous, inverting buck-boost converter. When the control MOSFET is on the voltage across the inductor, V_L is equal to the input voltage, V_{IN}. During this period, the current ramps up in the inductor. Also, the output capacitor sustains the output voltage. When the control MOSFET turns off and the sync MOSFET turns on the inductor current commutates, flowing through the system ground, the load, and through the sync MOSFET, generating a negative voltage across the load resistor with respect to system ground. The inductor current also charges the output capacitor, and the voltage across the inductor is equal to ($-V_{OUT}$).

APPLICATION NOTE

Designing an Inverting Buck-boost Converter with MagI³C Power Module WPMDH1302401 / 171032401
(6 - 42 V_{IN} / 3A / 5 - 24 V_{OUT})

3. Voltage, Current and Duty Cycle Limitations

Selecting the proper MagI³C Power module for buck topologies is straightforward – the input voltage range, output voltage range and output current range listed in each module´s datasheet show the precise limits for each of these quantities. For the inverting buck-boost more calculations are required, and both the maximum input voltage range and the output current range are lower when using this topology than they are for the buck.

3.1. Input Voltage Range

Closer inspection of the buck-boost regulator in Figure 3 reveals that the module´s reference voltage is no longer system ground, but in fact is the negative output voltage. The total voltage from the V_{IN} pin to the AGND pin of the module is equal to the input voltage plus the absolute value of the output voltage. This can be observed by considering that the voltages across C_{IN2} and C_{OUT} add together, with system ground at their midpoint. Table 1 shows the maximum input voltage rating for each member of the VDRM family:

Type	Package	Order Code	WE Part Description	V_{IN} [V]	V_{OUT} [V]	I_{OUT} [A]
Variable Step Down Regulator Module (VDRM)	TO263-7EP	171 012 401	WPMDH1102401J	6 - 42	5 - 24	1
	TO263-7EP	171 012 402	WPMDH1152401J	6 - 42	5 - 24	1.5
	BQFN-39	171 020 302	WPMDB1200362Q	2.95 6 V	0.8 - 3.6	2
	TO263-7EP	171 020 601	WPMDH1200601J	6 - 42	0.8 - 6	2
	BQFN-41	171 021 501	WPMDU1251501N	7 - 50	2.5 - 15	2.5
	TO263-7EP	171 032 401	WPMDH1302401J	6 - 42	5 - 24	3
	BQFN-39	171 040 302	WPMDB1400362Q	2.95 6 V	0.8 - 3.6	4
	TO263-7EP	171 050 601	WPMDM1500602J	6 - 36	0.8 - 6	5
	BQFN-39	171 060 302	WPMDB1600362Q	2.95 6 V	0.8 - 3.6	6

Table 1: Input voltage, output voltage and output current ranges for the VDRM MagI³C Power modules

So for example the 171 032 401 (42 V_{IN} / 3 A / 5 to 24 V_{OUT}) when operating at an input of 24 V would be limited to a theoretical maximum output voltage of -18 V. In practice at least 3 V to 4 V of headroom should be left for ringing and transients, so the recommended maximum output voltage for an input of 24 V would be around 14 V to 15 V.

Buck-boost operation also has a distinctive advantage over the buck regulator: as the name implies, the absolute value of the output voltage can be higher or lower than the input voltage. As long as the minimum on-time and off-time of the modules are respected, an output of -12 V is possible from an input as low as 6 V. Furthermore, once the module is operating the input voltage can go even lower than the normal, buck-mode minimum V_{IN} of 6 V as long as the sum of (V_{IN} + |-V_{OUT}|) is greater than or equal to 6 V. Figure 5 shows maximum input voltage as a function of the output voltage and also maximum output voltage as a function of input voltage.

APPLICATION NOTE

Designing an Inverting Buck-boost Converter with MagI³C Power Module WPMDH1302401 / 171032401
(6 - 42 V_{IN} / 3A / 5 - 24 V_{OUT})

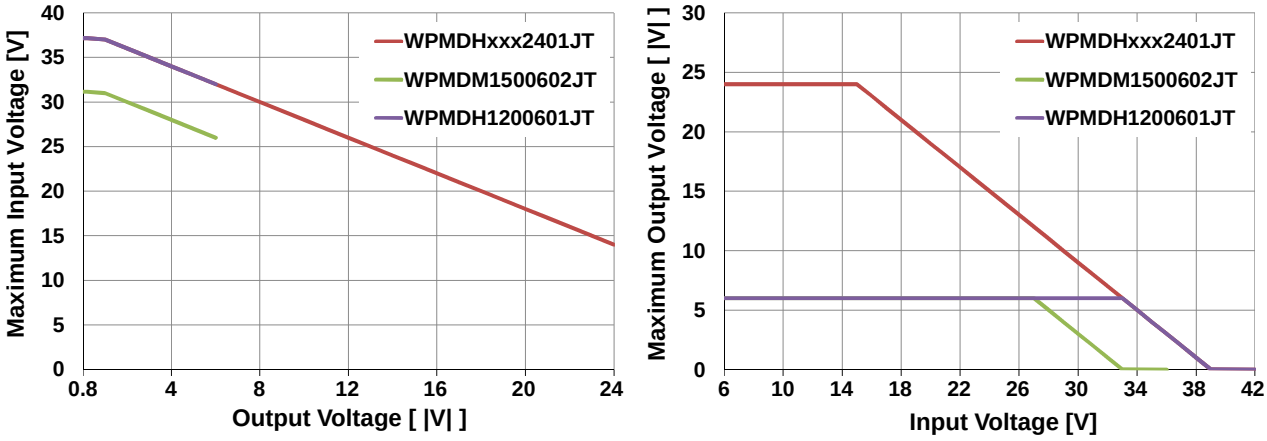

Figure 5: Graphical maximum input voltage and output voltage relationships

3.2. Maximum Output Current

In the buck-boost topology the maximum output current that the regulator can deliver is a function of the duty cycle. (It can also be considered to be a function of the ratio of input voltage to output voltage.) This is because MagI³C Power modules sense inductor current, and in the buck-boost topology the average value of inductor is not the same as the average value of the output current, as shown in EQ.1. Furthermore, MagI³C Power modules sense inductor current during the high side MOSFET on-time, when the current reaches its peak value. The over-current protection circuit monitors this peak inductor current. In order to calculate peak current the average current must first be determined. Average inductor current is a function of duty cycle (D) defined by:

$$I_{L\text{-}AVG} = \frac{I_{OUT}}{1 - D} \qquad \textbf{EQ.1}$$

$$D = \frac{|V_{OUT}|}{V_{IN} + |V_{OUT}|} \qquad \textbf{EQ.2}$$

The low voltage drops across the power MOSFETs and the internal power inductor can be ignored because they are small in comparison to $-V_O$ and V_{IN} for the majority of applications. In order to calculate the maximum possible output current for the buck-boost the output voltage minimum input voltage, inductance and switching frequency are needed. First, maximum duty cycle is calculated.

$$D_{MAX} = \frac{|V_{OUT}|}{V_{IN,min} + |V_{OUT}|} \qquad \textbf{EQ.3}$$

Each MagI³C Power module has a fixed over-current protection threshold – for convenience these limits along with the internal power inductors are listed in Table 2.

APPLICATION NOTE

Designing an Inverting Buck-boost Converter with MagI³C Power Module WPMDH1302401 / 171032401
(6 - 42 V_{IN} / 3A / 5 - 24 V_{OUT})

Part Number	Minimum Current Limit, I_{OCP} [A]	Internal Inductance, L1 [µH]
WPMDH1200601JT	2.3	10
WPMDM1500602JT	5.4	3.3
WPMDH1102401JT	1.5	15
WPMDH1152401JT	2.4	15
WPMDH1302401JT	3.2	10

Table 2: Minimum over-current protection threshold over the full temperature range

Peak-to-peak inductor ripple current and peak current for buck-boost regulators are calculated as follows:

$$\Delta i_L = \frac{V_{IN,min} \cdot D_{max}}{L_1 \cdot f_{SW}} \quad \textbf{EQ.4}$$

$$I_{L\text{-}PK} = I_{L\text{-}max} + \frac{\Delta i_L}{2} \quad \textbf{EQ.5}$$

Finally, the equations can be rearranged to show the maximum achievable output current for a given set of conditions:

$$I_{OUT\text{-}max} = (1 - D_{max}) \cdot \left(I_{OCP} - \frac{V_{IN,min} \cdot D_{max}}{2 \cdot L_1 \cdot f_{SW}} \right) \quad \textbf{EQ.6}$$

3.3. Duty Cycle Limits

The duty cycle in the VDRM family of MagI³C Power modules is not directly limited due to the constant on-time control, but the high side switch must turn off for at least 260 ns during each switching cycle and must stay on for at least 150 ns during every switching cycle. These limits create an effective minimum and maximum duty cycle that the modules can achieve for all topologies, and in all topologies, the limits become more and more restrictive as switching frequency increases. In general, the buck-boost is more likely to run into the maximum

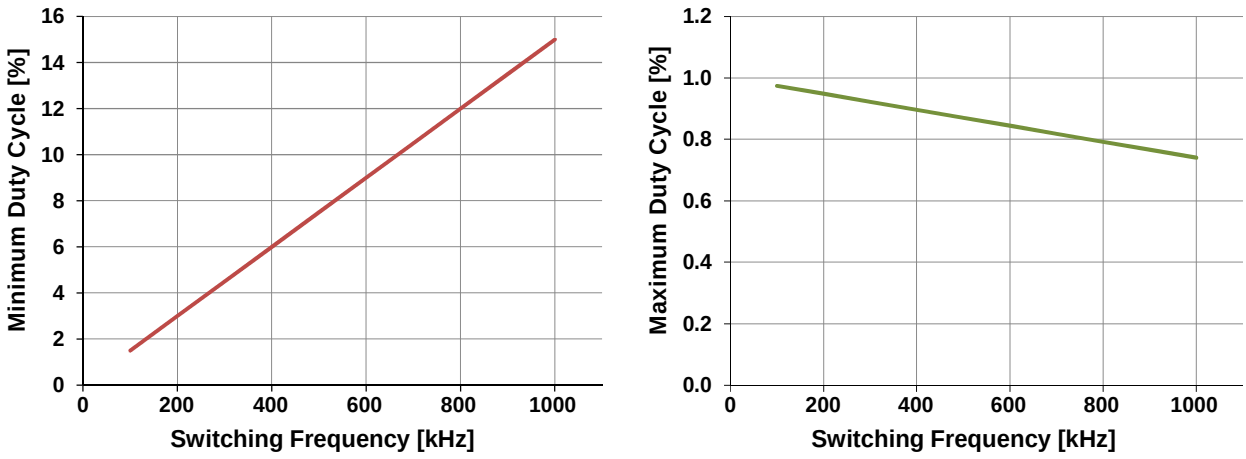

Figure 5: Duty cycle limits vs. switching frequency from 100 kHz to 1 MHz

APPLICATION NOTE

Designing an Inverting Buck-boost Converter with MagI³C Power Module WPMDH1302401 / 171032401
(6 - 42 V_{IN} / 3A / 5 - 24 V_{OUT})

duty cycle/minimum off-time limits than the buck because the buck-boost can operate with lower input voltages than a buck regulator.

4. Design Guide

This section will guide the user through the design and external component selection of an inverting buck-boost regulator meeting the following specifications:

Input Voltage: V_{IN} = 10 VDC to 28 VDC
Output Voltage: V_{OUT} = -12.0 VDC, I_{O-MAX} = 1.0 A
Estimated Power Efficiency, η = 90%

This converter can operate from 12 VDC or 24 VDC power inputs, rectified 12 VAC inputs, 12 V and 24 V batteries. The -12 V output could be used to power amplifiers, sensors or other analog functions that require a negative voltage.

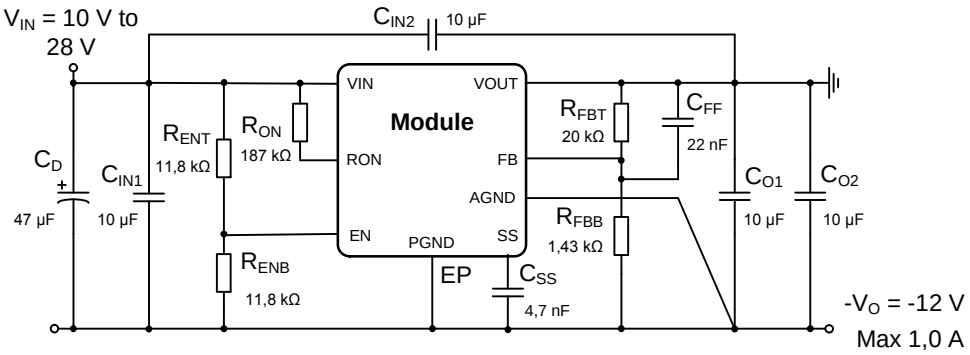

Figure 6: Circuit schematic for the design example

4.1. Selecting the Right Power Module

This process will often require some iteration. To start, the maximum voltage that will be applied from the V_{IN} pin to the V_{OUT} pin is (28 V + 12 V) = 40 V, so the 5 A MagI³C-VDRM module with its 36 V limit can be discarded. Then, average inductor current can be calculated using EQ.1 and EQ.3. Keep in mind that the highest current occurs when input voltage is at a minimum:

$$D_{max} = \frac{|V_{OUT}|}{V_{IN,min} + |V_{OUT}|} = \frac{12\ V}{10\ V + 12\ V} = 0.55$$

$$I_{L\text{-}AVG} = \frac{I_{OUT}}{(1 - D_{max}) \cdot \eta} = \frac{1.0\ A}{(1 - 0.55) \cdot 0.9} = 2.45\ A$$

If average current is more than 2.0 A then the three members of the family that deliver 1.0 A, 1.5 A and 2.0 A of output current can also be discarded, leaving only the 3.0 A version of MagI³C-VDRM. This is the part that will be used.

4.2. Select the Switching Frequency

This is a fundamental choice that will affect the power efficiency and dissipation in the module. Since the power inductor is internal, the compromise of space/size vs. efficiency is not as relevant as it is with standard switching regulators. Therefore the selection criteria are power efficiency/dissipation, the size of the input and output capacitors, the peak ripple current (so as not to run into the over-current protection) and the existence of any sensitive frequency bands.

Because of the 150 ns minimum on-time requirement, the maximum possible switching frequency is calculated as follows:

$$f_{SW,max} = \frac{V_{OUT}}{150\ ns \cdot V_{IN,max}} = \frac{12\ V}{150\ ns \cdot 28\ V} = 2.9\ MHz \qquad \textbf{EQ.7}$$

2.9 MHz is far beyond the maximum range recommended for the 3 A MagI³C-VDRM, which is 200 kHz to 800 kHz, and in fact 2.9 MHz is far beyond the practical switching frequency for a MagI³C Power module that delivers 12 W of output power – see the "Power Dissipation" section for details on the dependence of power dissipation on frequency. 500 kHz is a much more reasonable choice, and will be used.

4.3. Check the Peak Current and Over-current Protection

As discussed in the "Maximum Output Current" section, the ratio of input voltage to output voltage and the switching frequency all affect the maximum output current. With the 3.0 A module and the switching frequency selected, EQ.6 can be evaluated to make sure that the over-current protection will not engage:

$$I_{OUT\text{-}max} = (1 - D_{max}) \cdot \left(I_{OCP} - \frac{V_{IN,min} \cdot D_{max}}{2 \cdot L_1 \cdot f_{SW}}\right) = (1 - 0.55) \cdot \left(3.2\ A - \frac{10\ V \cdot 0.55}{2 \cdot 10\ \mu H \cdot 500\ kHz}\right) = 1.2\ A$$

Based upon this evaluation, the 3 A MagI³C-VDRM is an excellent choice.

4.4. Select the On-time Resistor, R_{ON}

The VDRM family of MagI³C Power modules uses a controlled on-time control system, and switching frequency is programmed by selecting a resistor that controls the time that the high-side MOSFET stays on each cycle. The on-time varies in inverse proportion to the input voltage to maintain a constant switching frequency over the input voltage range. For this reason, the selection equations are the same for buck and buck-boost regulators:

$$R_{ON} = \frac{V_{OUT}}{1.13 \cdot 10^{-10} \cdot f_{SW}} = \frac{12\ V}{1.13 \cdot 10^{-10} \cdot 500\ kHz} = 185\ k\Omega \qquad \textbf{EQ.8}$$

The closest E96 value is 187 kΩ, and once the actual R_{ON} value is selected, the maximum on-time should be evaluated for use in the next set of calculations:

$$t_{ON,max} = \frac{1.13 \cdot 10^{-10} \cdot R_{ON}}{V_{IN,min} + |V_{OUT}|} = \frac{1.13 \cdot 10^{-10} \cdot 187\ k\Omega}{10\ V + 12\ V} = 1.11\ \mu s \qquad \textbf{EQ.9}$$

4.5. Calculate the Internal Inductor Currents

Average inductor current is already known: from EQ.1 this is 2.45 A. Given the maximum on-time and the inductance the peak-to-peak ripple current and the peak inductor current can both be calculated:

$$\Delta i_L = \frac{V_{IN,min} \cdot t_{ON,max}}{L_1} = \frac{10\ V \cdot 1.11\ \mu s}{10\ \mu H} = 1.1\ A_{P\text{-}P} \qquad \textbf{EQ.10}$$

$$I_{L\text{-}PK} = I_{L\text{-}AVG} + \frac{\Delta i_L}{2} = 2.45\ A + \frac{1.1\ A}{2} = 2.99\ A \qquad \textbf{EQ.11}$$

APPLICATION NOTE

Designing an Inverting Buck-boost Converter with MagI³C Power Module WPMDH1302401 / 171032401
(6 - 42 V_{IN} / 3A / 5 - 24 V_{OUT})

4.6. Select the Output Capacitors

A target maximum for the peak-to-peak output voltage ripple must be defined first. If the loads do not specify their tolerance to ripple, values of 1-2% of the output voltage are typical. In this case, 1% of 12 V is 120 mV.

$$C_{O,min} = \frac{I_{O,max} \cdot t_{ON,max}}{\Delta v_{O\text{-}max}} = \frac{1.0\ A \cdot 1.11\ \mu s}{120\ mV} = 9.2\ \mu F \qquad \textbf{EQ.12}$$

$$ESR_{max} = \frac{\Delta V_{O\text{-}max}}{I_{L\text{-}PK}} = \frac{120\ mV}{2.99\ A} = 40\ m\Omega \qquad \textbf{EQ.13}$$

Unlike the smooth, low-RMS output of a buck converter, the buck-boost has a high-RMS, pulsating output current similar to the output of a boost or flyback converter. It is therefore very important to calculate the RMS current seen by the output capacitor(s):

$$I_{C_{OUT,RMS}} = I_{OUT,max} \cdot \sqrt{\frac{V_{OUT}}{V_{IN,min}}} = 1.0\ A \cdot \sqrt{\frac{12\ V}{10\ V}} = 1.1\ A \qquad \textbf{EQ.14}$$

In general, for values of capacitance less than approximately 20 µF it is possible to use purely ceramic capacitors without excessive cost. Furthermore, multi-layer ceramic capacitors (MLCCs) can withstand very high values of RMS current, making them an excellent choice for the output capacitors of buck-boost regulators. Keeping in mind the loss of capacitance of MLCCs when they operate with a DC bias, two 1210 size capacitors rated to 25 V and 10 µF each and an X7R dielectric will give about 7 µF each when the 12 V output voltage is applied across them. The typical ESR for such capacitors is around 2 to 3 mΩ, well below the calculated maximum, and hence the output voltage ripple will be much lower than the 120 $mV_{P\text{-}P}$ target.

4.7. Select the Input Capacitors

As with the output capacitors, the first step is to define a maximum for the input voltage peak-peak ripple. This value depends greatly upon the mechanical and electrical location of the buck-boost regulator within the application: when connected to the input power supply through a wiring harness, or in applications where regulations such as EN55025 define strict limits for conducted EMI the value for $\Delta vin\text{-}_{MAX}$ is defined precisely. In such cases, an additional L-C or ferrite-C filter is often needed to meet EMI regulations. (Note: more detailed information on filter design can be found in "Trilogy of Magnetics", available from Würth Elektronik.)

In the absence of set limits, a typical target is 1% of the minimum input voltage – in this case, 1% of 10 V is 100 mV. Input capacitance can then be calculated as:

$$C_{IN,min} = \frac{I_{OUT,max} \cdot t_{ON,max}}{\Delta V_{IN\text{-}MAX}} = \frac{1.1\ A \cdot 1.11\ \mu s}{100\ mV} = 11.1\ \mu F \qquad \textbf{EQ.15}$$

$$ESR_{MAX} = \frac{\Delta V_{IN\text{-}MAX}}{I_{L\text{-}PK}} = \frac{100\ mV}{2.99\ A} = 33\ m\Omega \qquad \textbf{EQ.16}$$

Buck-boost regulators pull high-RMS pulsating input currents just like buck regulators or flyback regulators, so again the calculation of input capacitor RMS current is critical:

APPLICATION NOTE

Designing an Inverting Buck-boost Converter with MagI³C Power Module WPMDH1302401 / 171032401
(6 - 42 V_{IN} / 3A / 5 - 24 V_{OUT})

$$I_{IN,AVG} = \frac{I_{OUT,max} \cdot V_{OUT}}{V_{IN,min} \cdot \eta} = \frac{1\,A \cdot 12\,V}{10\,V \cdot 0.9} = 1.33\,A \qquad \textbf{EQ.17}$$

$$I_{C_{IN,RMS}} = I_{IN,AVG} \cdot \sqrt{\frac{D_{max}}{1 - D_{max}}} = 1.33\,A \cdot \sqrt{\frac{0.55}{1 - 0.55}} = 1.47\,A \qquad \textbf{EQ.18}$$

4.7.1. Two Positions for the Input Capacitors

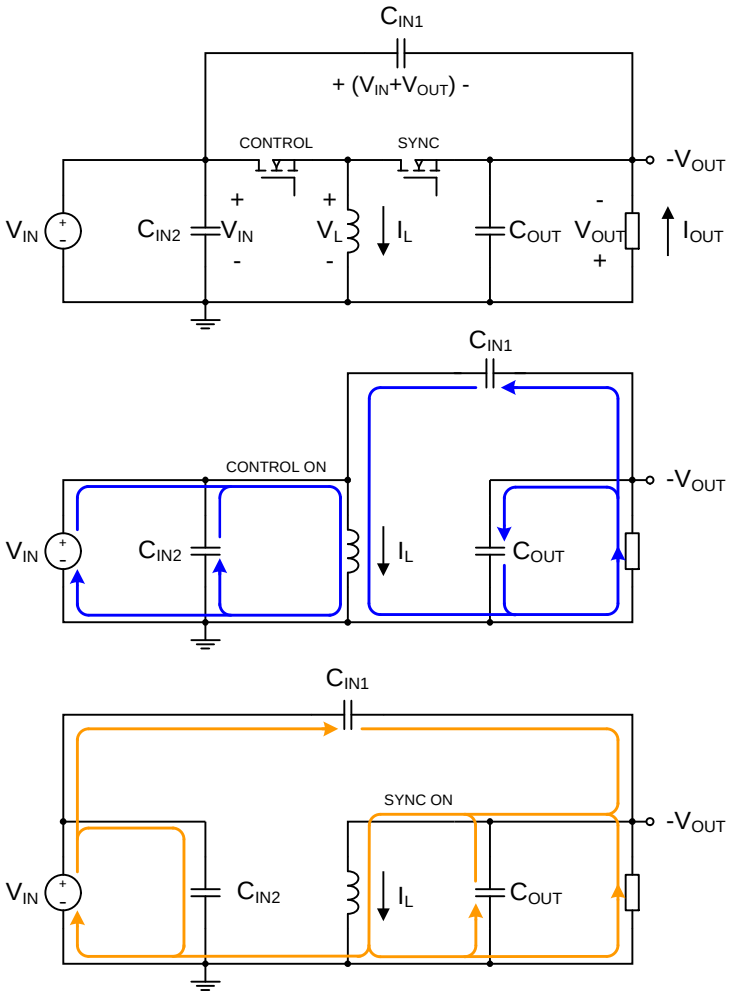

Figure 7: CIN1 is placed from V_{IN} to $-V_{OUT}$, CIN2 is placed from V_{IN} to GND, showing the current paths

Because of the way, the inverting buck-boost topology uses a buck regulator that is referenced to the negative output voltage there are two places where input capacitance is used. C_{IN2} is absolutely mandatory because it supplies the heavy AC currents drawn by the converter and it holds up the input voltage while the control MOSFET is off and the sync MOSFET is on, as shown in Figures 4 and 7. C_{IN1} is not strictly necessary, but it is very helpful for lowering the output voltage ripple, which reduces problems with loads that are sensitive to switching ripple such as amplifiers and ADC converters. Lower output ripple also improves conducted EMI at the output of the converter.

APPLICATION NOTE

Designing an Inverting Buck-boost Converter with MagI³C Power Module WPMDH1302401 / 171032401
(6 - 42 V_{IN} / 3A / 5 - 24 V_{OUT})

At first, C_{IN1} may appear to be an additional component and an additional cost to the BOM, but in practice this component can save both money and board area by reducing the size and cost or even eliminating output filters.

C_{IN1} sees an average voltage of (V_{OUT} + V_{IN}), and for this application the worst case is at $V_{IN,MAX}$ where the total reaches 40 V. C_{IN2} is the “standard” input capacitor placed from V_{IN} to system ground, so the maximum voltage is equal to $V_{IN,MAX}$ or 28 V in this example.

Balancing the total capacitance between positions C_{IN1} and C_{IN2} affects both the input voltage ripple (taken from V_{IN} to system ground, where conducted EMI is measured) and the output voltage ripple. In general, the best compromise comes from putting half of the total capacitance calculated in EQ.15 at C_{IN1} and the other half at C_{IN2}.

MLCCs are an excellent choice for the input capacitors for inverting buck-boost regulators due to the high-RMS currents seen by both C_{IN1} and C_{IN2}. The 40 V and 28 V maximum voltages seen by C_{IN1} and C_{IN2} respectively mean that a minimum of 50 V rated capacitors should be used, with X5R or X7R dielectrics. For this example 1210, X5R, 50 V rated 10 µF devices will be used. Despite the loss of capacitance due to DC bias, one advantage to designing with MLCCs is that the worst case where the most capacitance is needed is at the minimum input voltage where the capacitance loss is lowest. For this example at 22 V for C_{IN1} the actual capacitance is around 6 µF, and at 10 V for C_{IN2} the actual capacitance is around 9 µF. One capacitor will be placed at each position. Owing to the complex interaction and the difficulty of measuring currents through capacitors in the lab, a simulation can be very helpful. Figures 8 and 9 show the input voltage ripple with respect to ground and the output voltage ripples between two cases: all of the capacitance placed at C_{IN2} and then the recommended split of capacitance between the two positions.

In this example the input voltage ripple is similar between the two cases but is actually slightly higher when the capacitance is split between C_{IN1} and C_{IN2}. This is due to the capacitance loss from the application of (V_{OUT} + V_{IN}) across C_{IN1}. The dramatic improvement is in the output voltage ripple, and this comes from the continuous AC path that C_{IN1} provides from the input voltage to the output voltage. Without C_{IN1} there is no direct energy transfer from the input to the output during either of the two switching states, but with C_{IN1} AC current can flow, making the output ripple closer in both wave shape and amplitude to the desirable, low output voltage ripple of a buck converter.

APPLICATION NOTE

Designing an Inverting Buck-boost Converter with MagI³C Power Module WPMDH1302401 / 171032401

(6 - 42 V_{IN} / 3A / 5 - 24 V_{OUT})

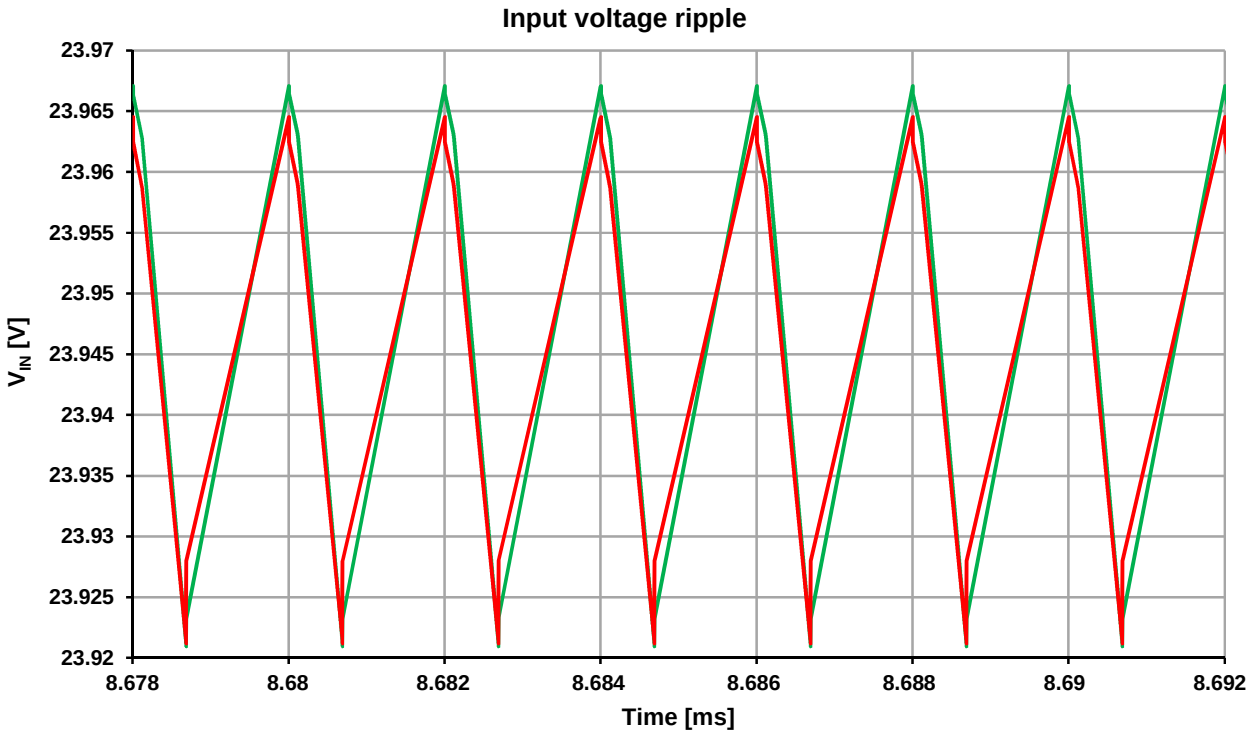

Figure 8: Input voltage ripple: all capacitance at C_{IN2} (red), 50-50 split of capacitance (green)

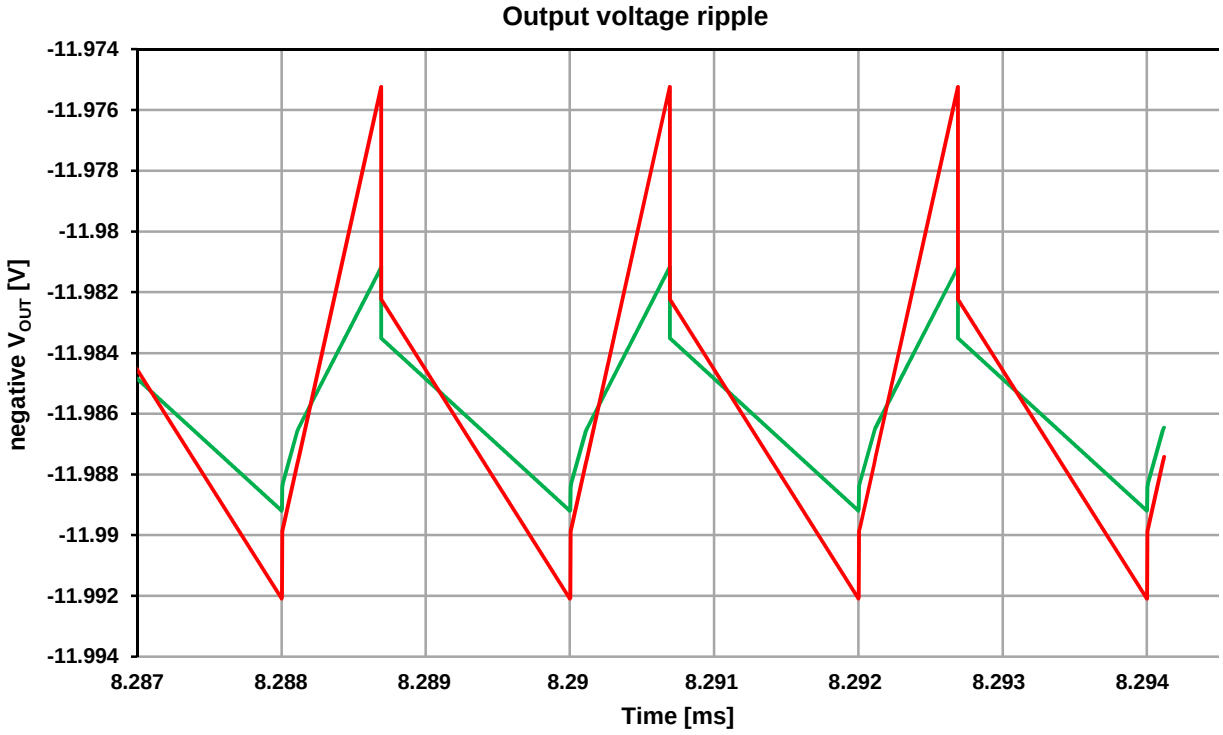

Figure 9: Output voltage ripple: all capacitance at C_{IN2} (red), 50-50 split of capacitance (green)

APPLICATION NOTE

Designing an Inverting Buck-boost Converter with MagI³C Power Module WPMDH1302401 / 171032401
(6 - 42 V_{IN} / 3A / 5 - 24 V_{OUT})

4.7.2. Damping to Prevent Resonance at the Input

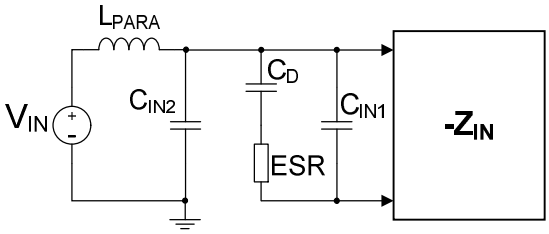

Figure 10: Parasitic input lead inductance L_{PARA}, input capacitors and damping capacitor C_D with controlled ESR

The combination of large parasitic inductance from long input supply leads and purely ceramic input capacitors creates a high quality factor L-C filter that can oscillate when it feeds the negative input impedance of a switching converter. From a mathematical perspective a switching power supply will resonate with the input filter whenever the impedance of the input filter is higher than the absolute value of the switcher´s negative input impedance. This sub-harmonic resonance is often called “power supply interaction”, and Figure 11 shows the adverse effect on the example circuit being designed in this application note when connected to the input power supply with 30 cm leads. The worst case for power supply interaction is at the minimum input voltage and maximum output current, where the absolute value of the converter´s input impedance is lowest. This oscillation at approximately 43 kHz is a source of EMI and should be eliminated by adding a larger capacitor with higher ESR in parallel with C_{IN1} to damp out the resonance.

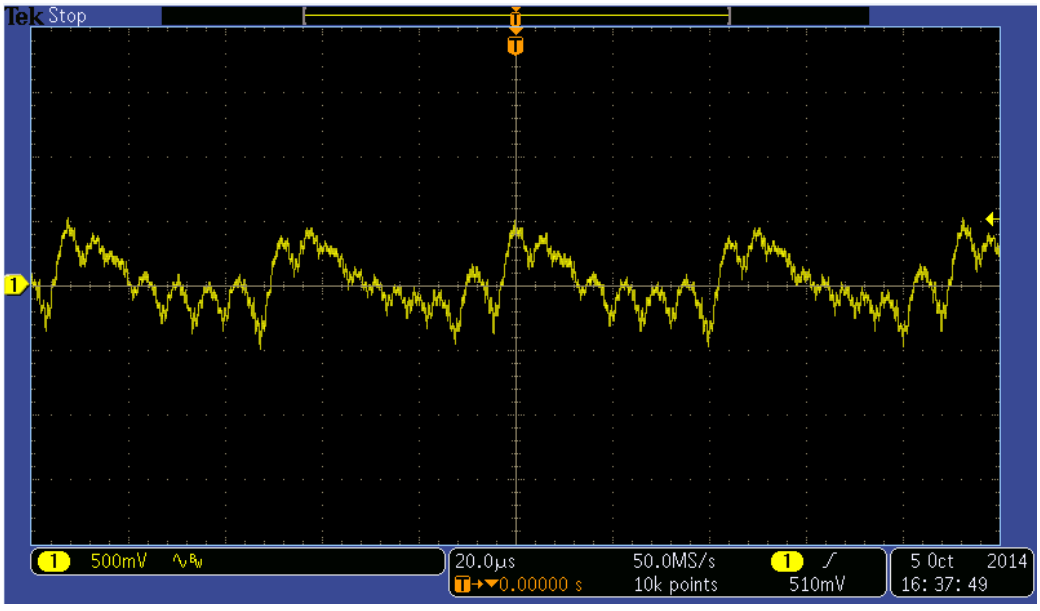

Figure 11: Input voltage with sub-harmonic oscillation due to power supply interaction when V_{IN} ≤ 10.5 V, I_O = 1,0A

The damping capacitor C_D should be 4-5 times greater in capacitance than the ceramic capacitor C_{IN1}, and in order to critically damp, the L-C resonance the minimum ESR of the damping capacitor can be calculated as:

$$ESR \geq \frac{1}{2} \cdot \sqrt{\frac{L_F}{C_{IN,1}}} - DCR = \frac{1}{2} \cdot \sqrt{\frac{1\,\mu H}{10\,\mu F}} - 0.003\,\Omega = 0.155\,\Omega \qquad \textbf{EQ.19}$$

For this example, the actual input inductance is purely parasitic, and in such cases, a value of 1 µH can be assumed. When an input inductor is used, this value is substituted for L_F. The ESR of most large MLCCs falls in the range of 2-3 mΩ and can be ignored. Aluminum capacitors are a good choice for damping due to their high ESR, but if necessary, a discrete resistor can be added in series with C_D in order to ensure enough damping resistance. For this example, assume that C_{IN1} has 100% of its rated capacitance when V_{IN} = 10 V (CIN1 = 10 µF). Therefore 47 µF provides the 4-5x capacitance needed. A 47 µF, 50V aluminum electrolytic capacitor with an impedance of 300 mΩ and rated to 500 mA of RMS current is an excellent choice. Not only will this capacitor damp any potential oscillation, it will also reduce both input voltage and output voltage peak to peak ripple.

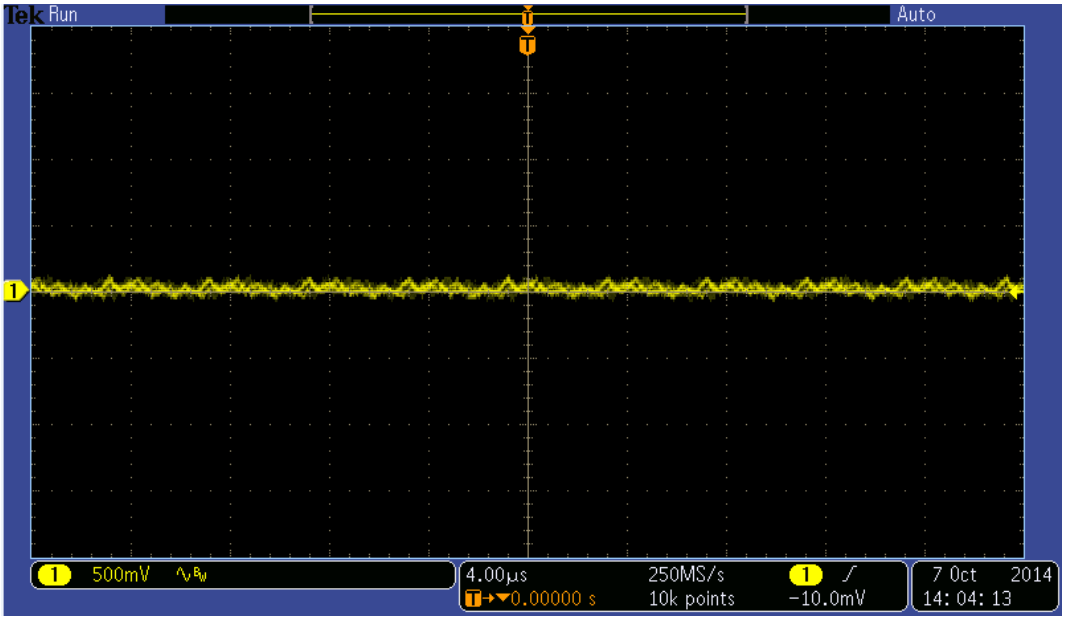

Figure 12: Input voltage ripple with damping capacitor C_D in parallel with CIN1. V_{IN} = 10,0 V, I_O = 1,0 A

4.8. Output Voltage, UVLO and Soft-start

Output voltage is selected with a resistor divider pair using the same equations as the buck regulator. Select a value for the top feedback resistor RFBT between 10 kΩ and 50 kΩ. For this example, RFBT is 20 kΩ. Then the bottom resistor RFBB is calculated as:

$$R_{FFB} = \frac{R_{FBT}}{\frac{V_{OUT}}{0.804\ V} - 1} = \frac{20\ k\Omega}{\frac{12V}{0.804\ V} - 1} = 1.43\ k\Omega \quad (\text{Set } R_{FBB} = 1.43\ k\Omega) \qquad \textbf{EQ.20}$$

Soft-start is also unchanged. However, the input under-voltage lockout does require some changes. If a standard resistor divider is used extending from V_{IN} to $-V_O$ then the rising, enable threshold stays the same as for a buck regulator. This is because the $-V_O$ net is at approximately zero volts before the buck-boost starts up. However once the regulator begins operating the voltage at the module´s GND pin drops by the output voltage, shifting the falling UVLO threshold (the disable threshold) down by an amount equal to the output voltage. Care must be taken not to exceed the 6.5 V maximum operating voltage of the EN pin once the module is operating and the total voltage between the V_{IN} and GND pins equals (V_{IN} + V_{OUT}). The standard buck evaluation boards for the MagI³C Power modules include a 5.1 V zener diode connected from the EN pin to the GND pin to prevent overvoltage, and this zener diode should be included in all designs where UVLO is done with a simple resistor divider.

APPLICATION NOTE

Designing an Inverting Buck-boost Converter with MagI³C Power Module WPMDH1302401 / 171032401
(6 - 42 V_{IN} / 3A / 5 - 24 V_{OUT})

4.8.1. Level Shift Circuits for Precision UVLO or Logic Enable

In some applications the large hysteresis between the rising enable UVLO threshold (V_{EN}) and the falling, shutdown threshold (V_{SD}) can be an advantage, but in most cases the difference between V_{EN} and V_{SD} is less than one volt. In order to achieve a small hysteresis a level-shifting comparator is needed. Figure 13 shows one example built with low-cost parts.

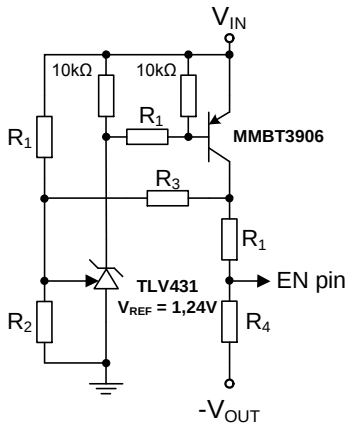

Figure 13: Level-shifting comparator for precision UVLO with controlled hysteresis

The following equations define the resistor values needed to set the desired UVLO thresholds:

$$\mathbf{V_{EN} = 9.5\ V \qquad V_{SD} = 9.0\ V}$$

$$R_1 = (V_{EN} - V_{REF}) \cdot 10\ k\Omega = (9.5\ V - 1.24\ V) \cdot 10\ k\Omega = 82.6\ k\Omega \qquad \textbf{EQ.21}$$

$$(\text{Set } R_1 = 82{,}5\ k\Omega)$$

The logic high enable voltage at the EN pin should be set to around 3 V.

$$R_4 = \frac{3\ V \cdot R_1}{V_{OUT} + V_{EN} - 3V} = \frac{3\ V \cdot 82.5\ k\Omega}{12\ V + 9.5\ V - 3\ V} = 13.4\ k\Omega \qquad \textbf{EQ.22}$$

$$(\text{Set } R_4 = 13.7\ k\Omega)$$

$$R_3 = \frac{R_1 \cdot (V_{SD} + V_{OUT})}{V_{EN} - V_{SD}} - R_1 - R_4 \qquad \textbf{EQ.23}$$

$$R_3 = \frac{82.5\ k\Omega \cdot (9\ V + 12\ V)}{9.5\ V - 9\ V} - 82.5\ k\Omega - 13.4\ k\Omega = 3.37\ M\Omega$$

$$(\text{Set } R_3 = 3.4\ M\Omega)$$

$$R_2 = \frac{R_1 \cdot V_{REF} \cdot (R_1 + R_3 + R_4)}{(R_1 + R_3 + R_4) \cdot (V_{EN} - V_{REF}) - R_1 \cdot (V_{OUT} + V_{REF})} \qquad \textbf{EQ.24}$$

$$R_2 = \frac{82.5\ k\Omega \cdot 1.24\ V \cdot (82.5\ k\Omega + 3.4\ M\Omega + 13.7\ k\Omega)}{(82.5\ k\Omega + 3.4\ M\Omega + 13.7\ k\Omega) \cdot (9.5\ V - 1.24\ V) - 82.5\ k\Omega \cdot (12\ V + 1.24\ V)} = 12.9\ k\Omega$$

$$(\text{Set } R_2 = 13\ k\Omega)$$

APPLICATION NOTE

Designing an Inverting Buck-boost Converter with MagI³C Power Module WPMDH1302401 / 171032401
(6 - 42 V_{IN} / 3A / 5 - 24 V_{OUT})

Referencing the module to the -V_O net also changes the interface for a CMOS or TTTL logic level enable/shutdown from other ICs, microcontrollers, etc. A signal-level P-MOSFET and two resistors are required as shown in the left-hand image of Figure 3. RENT and RENB should both be set to 10 kΩ.

5. Using the Buck Evaluation Board for Inverting Buck-boost

Just a few steps and a soldering iron are needed to evaluate the MagI³C Power modules as buck-boost regulators. To create the circuit designed in Section 3, begin with the 3 A MagI³C-VDRM evaluation board. Then follow these steps:

1. The original input capacitors are two 1210, X5R, 50V, 10 µF MLCCs. Leave one in place as C_{IN1}, then remove the second, stand it up and connect it with the shortest wire possible to the former "V_{OUT}" node, which is now system ground. This will be C_{IN2}.
    - To prevent the sub-harmonic oscillation explained in Section 3.7.2, add an aluminum electrolytic capacitor rated to at least 47 µF, 50 V between the V_{IN} and -V_{OUT} nodes.
2. To move the enable (V_{IN} rising) threshold to 9.5 V, replace RENB with an 18 kΩ, 1% resistor. Keep in mind that the falling threshold will be shifted upwards by the 12 V of the output voltage, such that in practice the regulator will continue operating until the input voltage falls to near zero.
    - To use a logic enable: Remove RENT and connect a 12 kΩ through-hole resistor from V_{IN} to the source of a through-hole P-MOSFET. Connect the base to system ground, and the drain to the EN pin of the module.
    - To set the hysteresis as defined in Section 4.8.1, remove both RENT and RENB. Assemble the circuit of Figure 13 along with the calculated values on a small section of perforated PCB ("perfboard" or "dot PCB") and then connect it with the shortest wiring possible to the V_{IN}, GND, -V_O and EN nodes of the evaluation board.
3. Affix stickers or cross out the original "GND" marking and re-label it as "-V_{OUT}". Do the same for the original "V_{OUT}" marking and label it as "GND". Using a different colored hookup wire such as blue will help remind the user that the output voltage is negative.
    - Keep in mind that many electronic loads only work with positive voltages, so the system ground of the modified evaluation board should connect to the positive input of the e-load, and the negative output voltage of the evaluation board should connect to the negative input of the e-load.

APPLICATION NOTE

Designing an Inverting Buck-boost Converter with MagI³C Power Module WPMDH1302401 / 171032401 (6 - 42 V_{IN} / 3A / 5 - 24 V_{OUT})

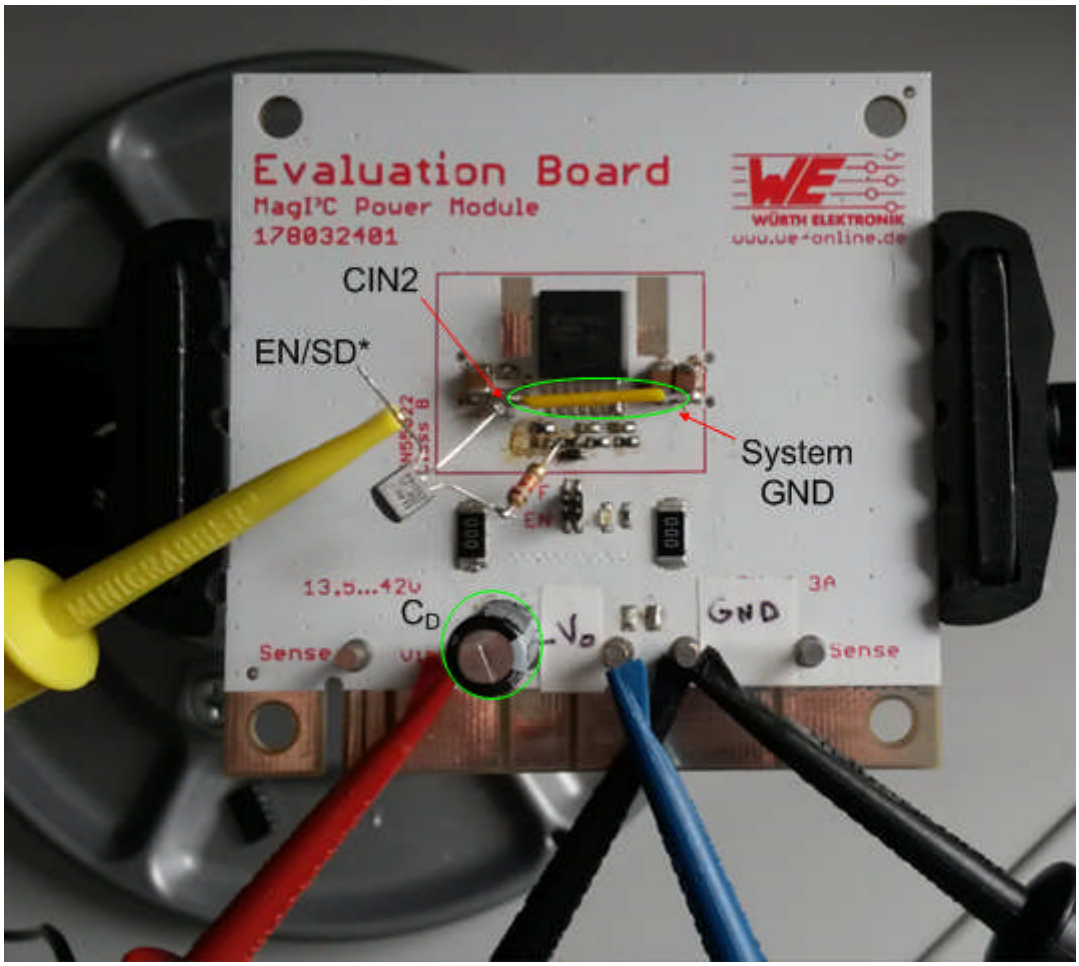

Figure 14: 178032401 evaluation board with modifications for use as an inverting buck-boost

6. Thermal Considerations

The theory from the 178 032 401 datasheet in the section titled “Power Loss and Board thermal Requirements” can be applied to the buck-boost regulator with a few changes. Start by reviewing the following two plots from the datasheet:

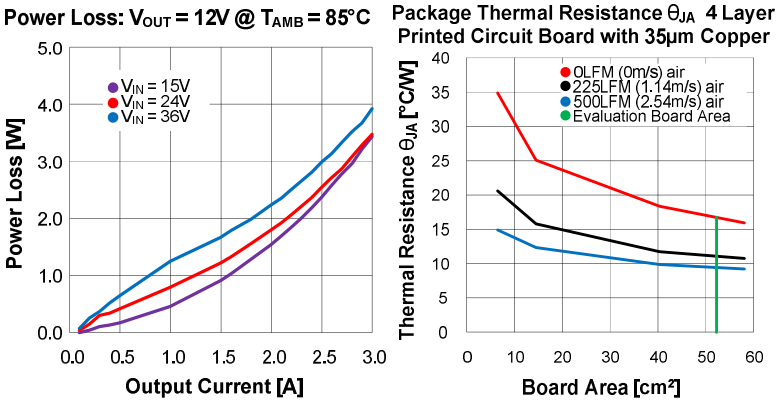

Figure 15: Thermal response data from the MagI³C Power Module - VDRM (171 032 401) datasheet

APPLICATION NOTE

Designing an Inverting Buck-boost Converter with MagI³C Power Module WPMDH1302401 / 171032401
(6 - 42 V_{IN} / 3A / 5 - 24 V_{OUT})

In order to use the curves from Figure 15, substitute the inductor current $I_{L\text{-}AVG}$ calculated in EQ.1 for output current. The worst case for power dissipation is when input voltage is lowest and therefore inductor current is highest. Substitute ($V_{IN,MIN}$ + |V_{Out}|) for V_{IN} in the curve of Power Loss vs. Output Current. For this example, (10 V + 12 V) = 22 V, so the red curve for V_{IN} = 24 V is closest. Recalling that the average inductor current is 2.45 A, the power dissipation, P_D read from the curve is approximately 2.5 W. From the datasheet, the maximum thermal resistance needed to keep the module´s die temperature below the limit of 125 ºC is:

$$\theta ja_{MAX} = \frac{T_{J_{max}} - T_A}{P_D} = \frac{125\,°C - 85\,°C}{2.5\,W} = 16\,\frac{°C}{W} \qquad \textbf{EQ.25}$$

The curve of Thermal Resistance vs. Board Area shows that approximately 55 cm² is needed to dissipate this much power and keep the module temperature within the 125ºC limit.

7. Bill of Materials

Index	Description	Size	Value	Order Code
U_1	MagI³C Power Module	7 PIN VDRM	U_{In}: 6 - 42 V, U_{Out}: 0,8-6 V,I_{Out}: 3 A	171 032 401
C_{IN1}, C_{IN2}, C_{OUT1}, C_{OUT2}	Multi-layer Ceramic Capacitor	1210	10 µF, 50 V, +/-20%, X5R	
C_D	Aluminum electrolytic capacitor	8 x 11.5 mm	100 µF, 0.87 A, 0,3 Ω	EEUFR1H101
C_{SS}	Multi-layer Ceramic Capacitor	0603	4,7 nF, 50 V, +-10%, X5R	
R_{ENB}, R_{ENT}	Thick Film Resistor	0603	11.8 kΩ, 1%	
R_{FBB}	Thick Film Resistor	0603	1.43 kΩ, 1%	
R_{FBT}	Thick Film Resistor	0603	20 kΩ, 1%	
R_{ON}	Thick Film Resistor	0603	187 kΩ, 1%	

8. PCB Layout

The following section provides a step-by step guide to PCB layout for best efficiency, thermal management and electromagnetic compatibility (EMC). Figure 16 shows the complete schematic, including optional input and output filters for other circuit configurations or requirements.

APPLICATION NOTE

Designing an Inverting Buck-boost Converter with MagI³C Power Module WPMDH1302401 / 171032401
(6 - 42 V_{IN} / 3A / 5 - 24 V_{OUT})

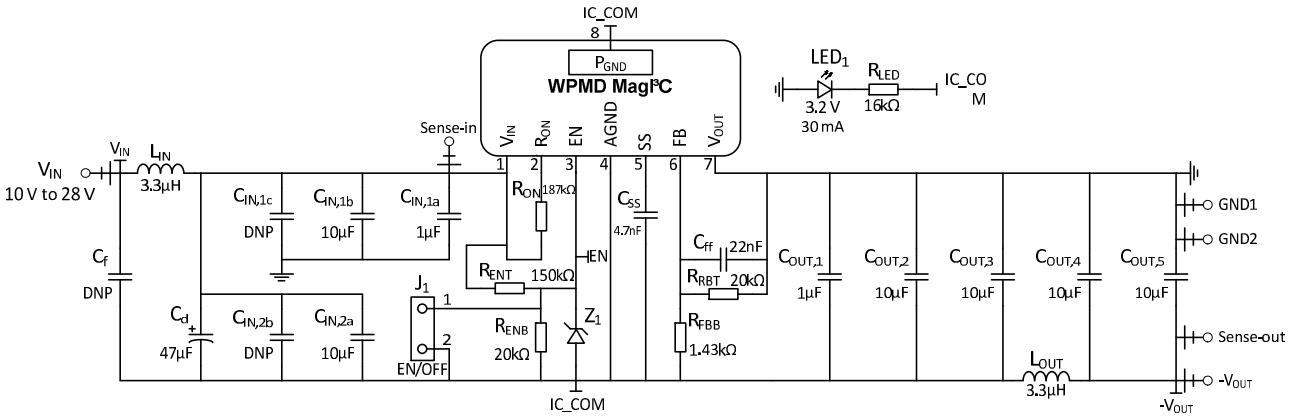

Figure 16: Complete circuit schematic for PCB layout

One optional component not represented on this schematic is a heatsink for the MagI³C module, a Fischer FK 244 08 D PAK heatsink. The 3.5 mm x 9 mm top layer pads on either side of the module (seen in Figures 17 and 18) are for mounting of this heatsink.

8.1. Place the Module and the Ceramic Input Capacitors

8.1.1. Switching Frequency and "Ringing" Frequency

In general, there are two fundamental noise frequencies in hard switched converters: the switching frequency and the "ringing" frequency. "Ringing" refers to the oscillation that occurs when energy stored in the parasitic capacitance of semiconductor switches releases during the switch openings and closings and then rings with the parasitic inductance present in the circuit. Ringing typically occurs at frequencies that are several orders of magnitude higher than the switching frequency, usually in the range of 50 MHz to 200 MHz. The current loop with the highest electrical noise (electromagnetic interference, EMI) is the one connecting the input capacitor(s) to the internal power MOSFETs of the MagI³C Power modules, so minimizing the area enclosed by this loop is critical for keeping radiated EMI as low as possible. Place the smallest capacitors closest to the pins/pads of the module where they can be most effective in filtering the ringing. In this context, "smaller" refers both the capacitance of the part and their physical size. The higher the frequency of a signal the more efficiently it radiates with decreasing loop size. Therefore lower capacitance will filter higher frequencies more effectively. Just as important is the physical size of the capacitors because the smaller the device is the lower its parasitic inductance (ESL), and that also makes the physically smaller capacitor a better filter of higher frequency noise.

8.1.2. Routing the Two Input Loops

For the inverting buck-boost there are two input loops: one between V_{IN}, the power switches and GND, and the other between V_{IN}, the power switches and $-V_O$. A compromise is needed, and priority should be given to the V_{IN}-Switches-V_O loop because it carries heavier peak-to-peak ripple current and therefore radiates more EMI than the V_{IN}-Switches-GND loop.

APPLICATION NOTE

Designing an Inverting Buck-boost Converter with MagI³C Power Module WPMDH1302401 / 171032401 (6 - 42 V_{IN} / 3A / 5 - 24 V_{OUT})

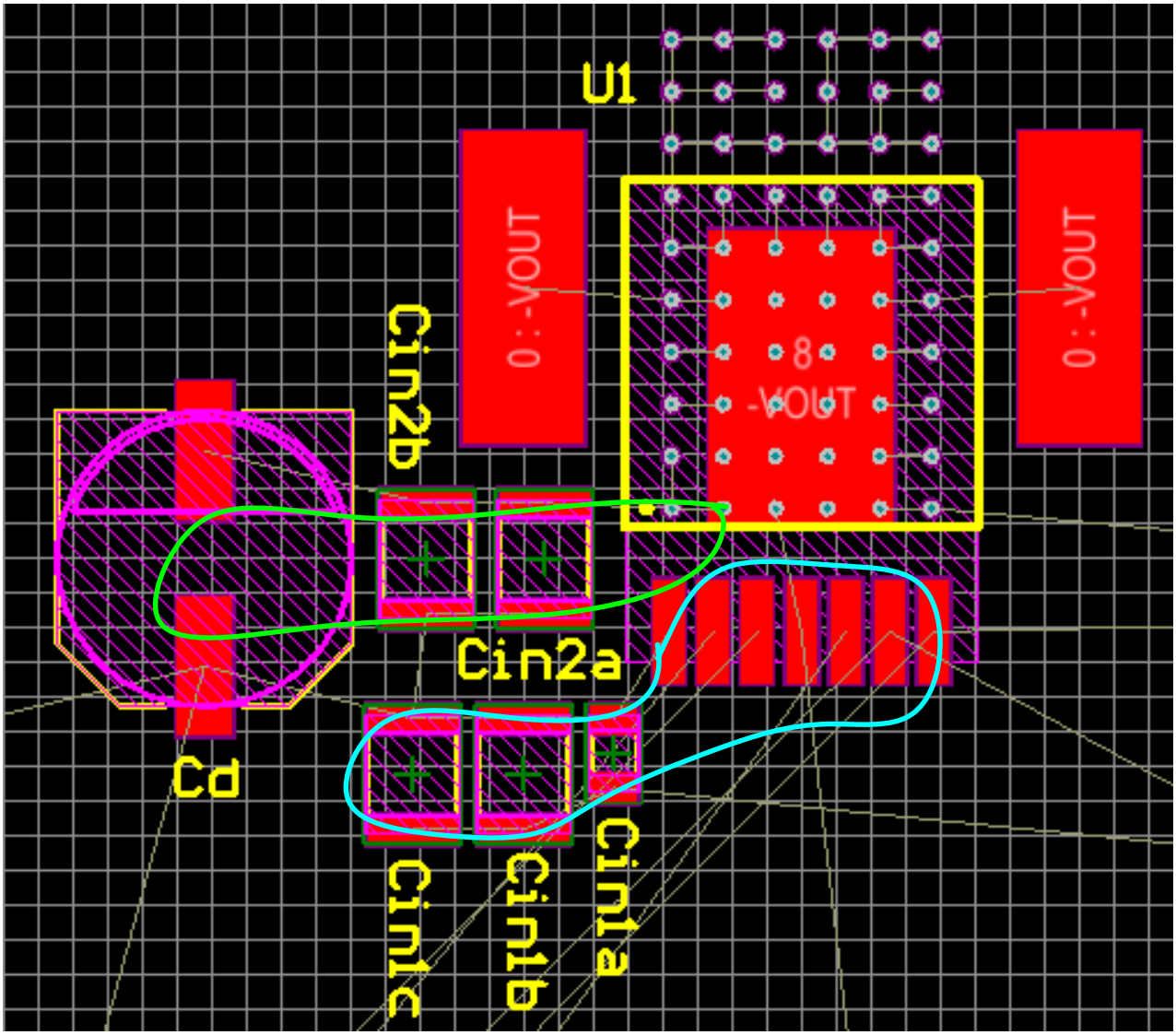

Figure 17: Place the input capacitors in the smallest possible loops, right next to the pins/pads of the module. The V_{IN}-Switches-V_O loop is in green and the V_{IN}-Switches-GND loop is in blue

8.1.3. Place Larger, Higher Capacitance Capacitors Farther Away

Capacitor C_d provides input filter damping and also reduces the ripple current/voltage at the switching frequency. It can be placed farther away from the module because it is a higher capacitance device with much higher ESL and therefore it has little effect on the high frequency EMI.

8.2. Place the Output Capacitors and the Input/Output Filters

The output capacitors in the buck-boost topology filter a discontinuous, high-RMS current just like the input capacitors. They should include a mixture of smaller and larger ceramic devices to filter both the high frequency ringing and the low frequency switching and noise. As with the input, the smallest devices should go in closest to the pins/pads of the module, followed by the larger ceramic capacitors and finally any bulk capacitors (aluminum electrolytic, polymer aluminum, tantalum, etc). The input filter (L_{IN} and C_F) and the output filter (L_{OUT}

and C_{04}-C_{05}) are both optional – by default neither filter´s components are installed – but when they are used they should be placed farther out from the module. Both filters act on the noise generated at the switching frequency and the harmonics of the switching frequency, hence it is important to route them so that all of the input current coming from the input power supply and all of the output current going out through the output connectors flows through the pads of the filter capacitors C_F and C_{04}-C_{05}.

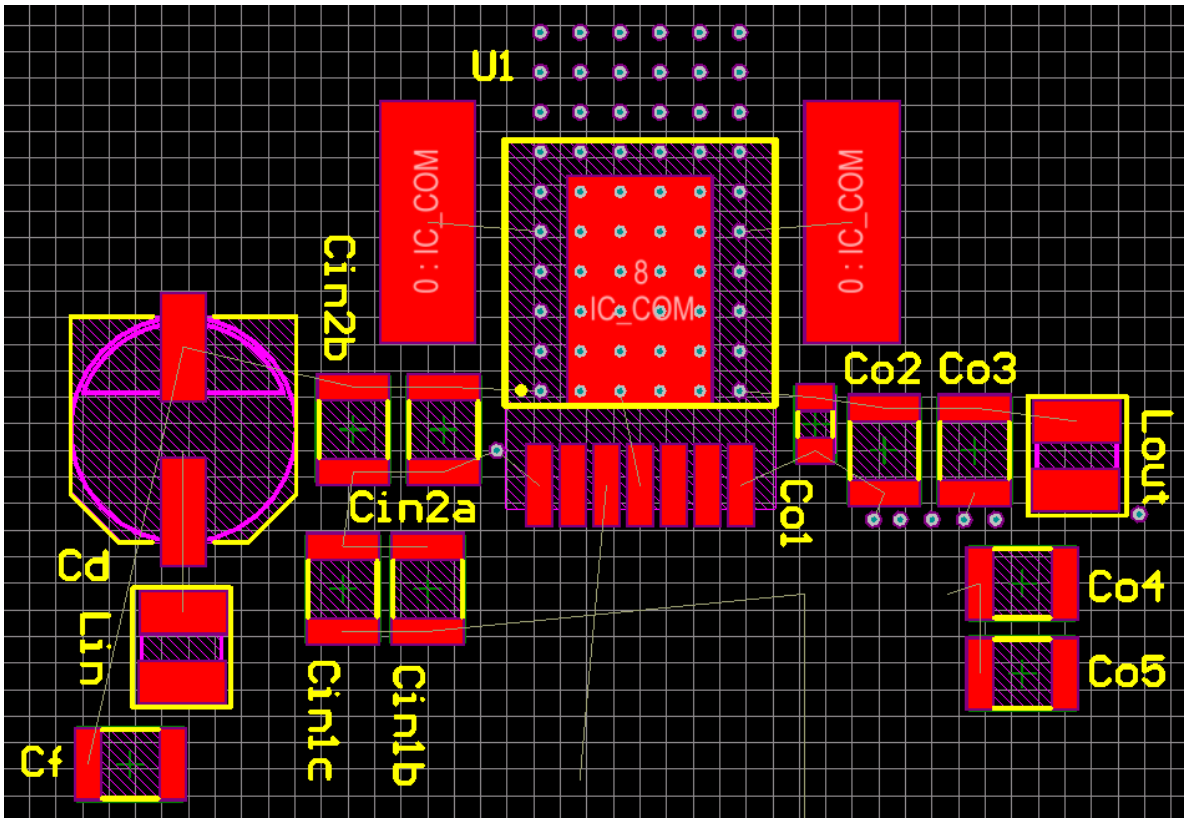

Figure 18: The output capacitors and L-C filters for the input and output of the converter

8.3. Place the Analog Components

In this case, “analog” refers to all the components that set the analog functions of the MagI³C Power modules, such as the output voltage, the UVLO threshold and the soft-start time. In this case these components should all go in close to the pins of the module, but the reason is different: By minimizing the length of the connections and the loop area between the analog components and the pins of the module their susceptibility to EMI generated by the power switches, the inductor and any external noise sources is minimized.

8.3.1. Place the Output Voltage Resistor Divider Close to the Module

One common layout error is placement of the output feedback resistive divider (Rfbt and Rfbb) close to the final output capacitor (C_{03} or C_{04}, depending upon the use of the output filter.) This is a mistake because the high impedance of the trace connecting the midpoint of the divider to the FB pin is of very high impedance – it´s the input to a comparator or an operational amplifier. The high impedance makes this trace very susceptible to noise pickup. Instead, minimize this trace by keeping Rfbt and Rfbb just as close to the FB pin and the AGND pin as possible.

APPLICATION NOTE

Designing an Inverting Buck-boost Converter with MagI³C Power Module WPMDH1302401 / 171032401 (6 - 42 V_{IN} / 3A / 5 - 24 V_{OUT})

8.3.2. Use a Single-Point Reference for the Analog Components

Another useful technique is to route all of the analog components that connect to the AGND pin of the module with one top-layer trace or copper shape, and then connecting that shape to the AGND pin at only one point. (Note that electrically the AGND pin is connected to the -V_O node prior to the output filter. In the schematic of Figure 16 this net is referred to as “IC_COM”.) A short trace will then connect the AGND pin to the thermal pad of the module, which is analogous to the “PGND” or “Power Ground” pins of standard switching regulator or controller ICs. This single point connection helps maintain a common reference voltage for all of the analog functions. Even if electrical noise is picked up by the AGND trace or shape, the relative reference voltage between the MagI³C Power module and the analog components will stay the same.

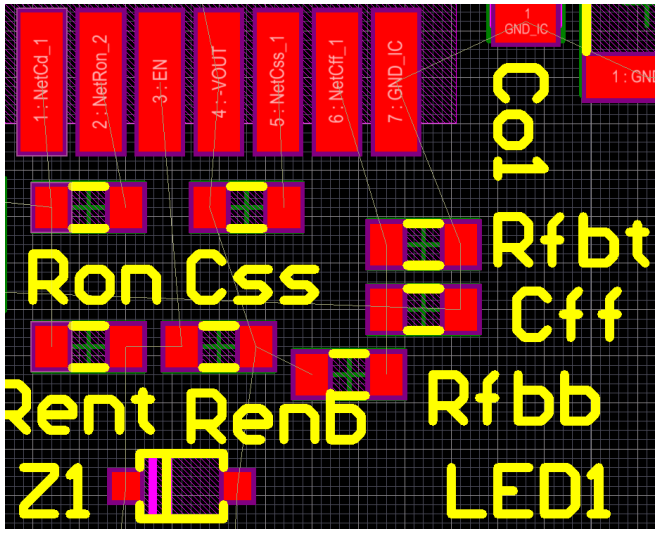

Figure 19: Placement of the analog components, with detail in the plot on the right

APPLICATION NOTE

Designing an Inverting Buck-boost Converter with MagI³C Power Module WPMDH1302401 / 171032401 (6 - 42 V_{IN} / 3A / 5 - 24 V_{OUT})

8.4. Route the Top Layer Power Polygons

The high current paths that carry the input and output current and connect the input and output capacitors should use wide traces or solid shapes. For devices with high power density like the MagI³C Power modules the copper shape connected to the power pad and pin 4 of the device is also the main path for heat to dissipate. Note that for the inverting buck-boost regulator this net is the negative output voltage, $-V_O$ prior to the output filter, labelled "IC_COM". Routing the power shapes close to one another between nets such as V_{IN} and GND, $-V_O$ and GND and V_{IN} and $-V_O$ increases the beneficial parasitic capacitance between them, and this typically adds 100 pF to 1 nF that is very helpful for filtering the highest frequencies of EMI.

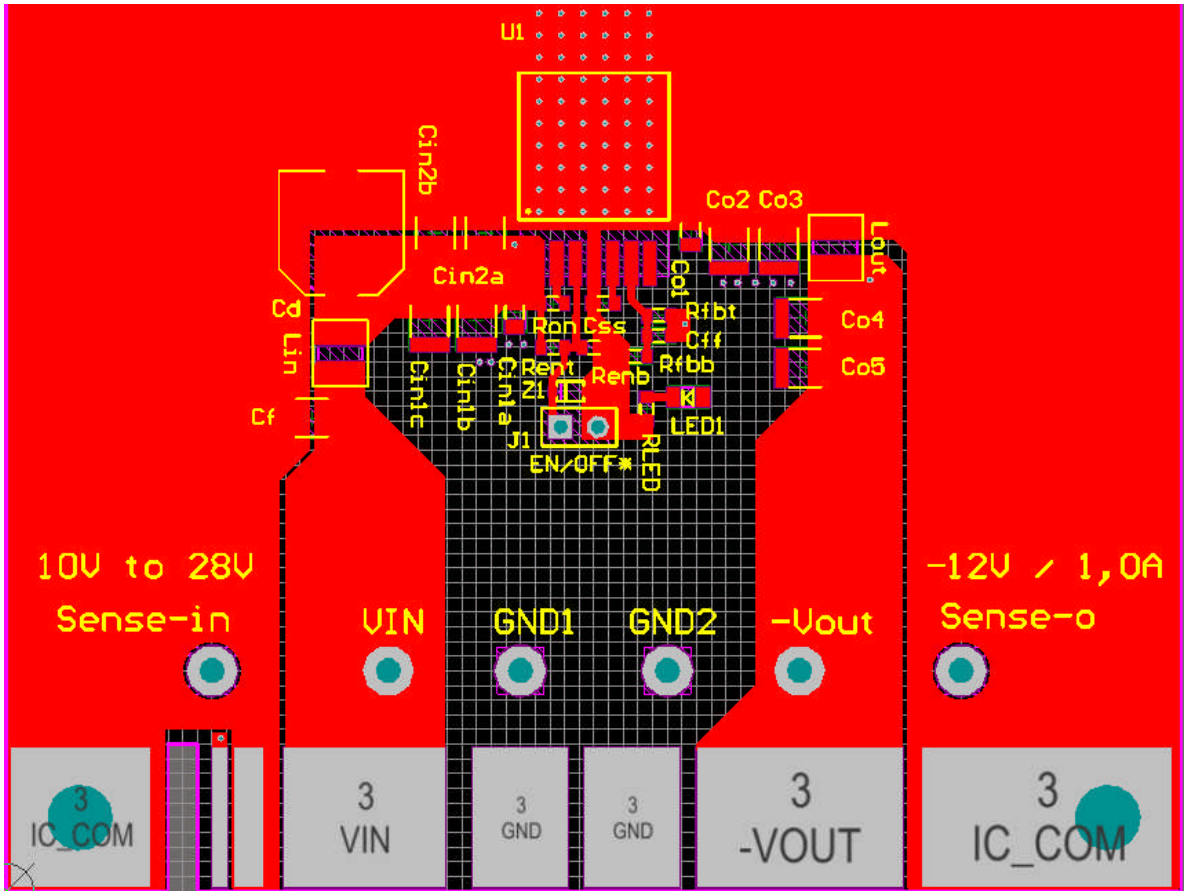

Figure 20: V_{IN}, IC_COM and $-V_O$ power polygons

APPLICATION NOTE

Designing an Inverting Buck-boost Converter with MagI³C Power Module WPMDH1302401 / 171032401
(6 - 42 V_{IN} / 3A / 5 - 24 V_{OUT})

8.5. Route the Analog Components Before the GND Polygon

Begin by placing the reference trace or shape as discussed in the “Place the Analog Components” section and shown in Figure 19.

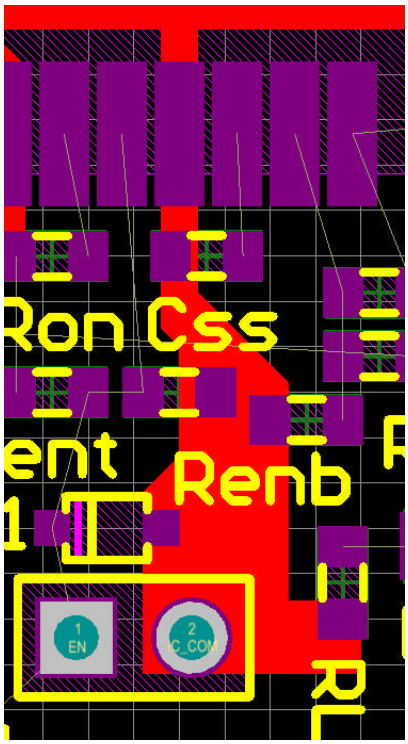

Figure 21: Single-point connection of all the analog components to the AGND pin and then to the power pad

APPLICATION NOTE

Designing an Inverting Buck-boost Converter with MagI³C Power Module WPMDH1302401 / 171032401
(6 - 42 V_{IN} / 3A / 5 - 24 V_{OUT})

8.6. Route System GND

For this buck-boost converter, the GND net carries an important link on the bottom layer between the negative connections of the input capacitors and the positive connections of the output capacitors. This shape helps to lower inductance in the V_{IN}-Switches-GND loop. In general any paths that carry switching currents should be routed without changing layers or using vias because the vias introduce unwanted resistance and, even worse, added inductance. When it is absolutely necessary, use multiple vias in parallel to reduce both the resistance and the inductance.

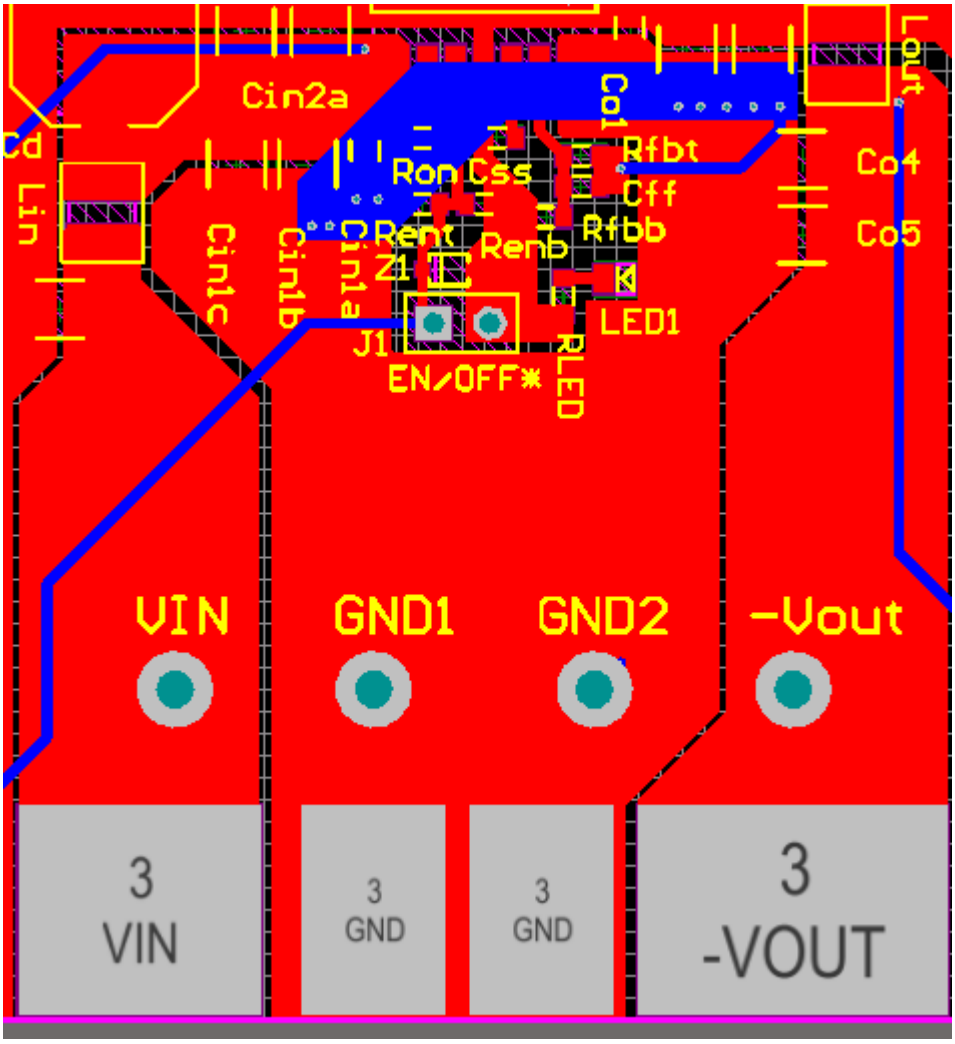

Figure 22: GND net routed on the top and bottom layers

APPLICATION NOTE

Designing an Inverting Buck-boost Converter with MagI³C Power Module WPMDH1302401 / 171032401 (6 - 42 V_{IN} / 3A / 5 - 24 V_{OUT})

8.7. Flood the Bottom Layer for Thermal Management

The power pad of the module is connected to the IC_COM net, so the maximum area on the bottom layer should be connected to this net. It is important to keep the bottom layer as solid as possible for both electrical purposes (more beneficial parasitic capacitance between V_{IN} and GND and between V_{IN} and $-V_{OUT}$) and for thermal management (more copper area connected through the thermal vias to the exposed pad). Only the short connection on the GND net and a minimum number of Kelvin sense lines are routed on this layer, and then the rest should be flooded with copper connected to IC_COM.

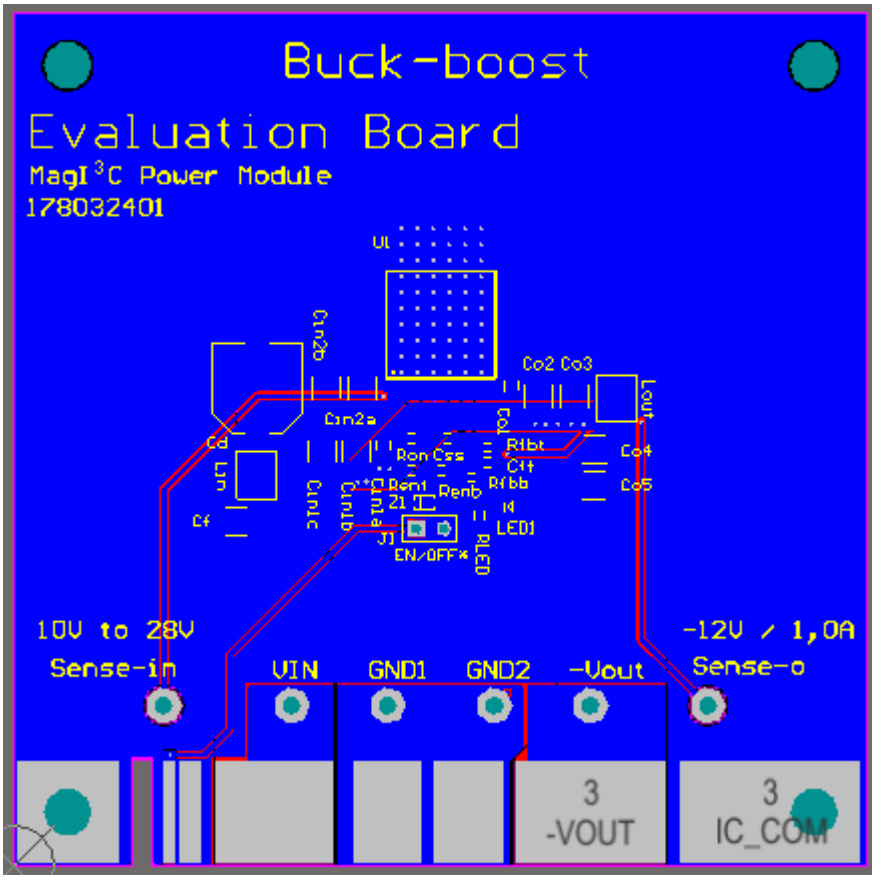

Figure 23: Bottom layer showing solid plane connected to IC_COM with multiple thermal vias

9. Conclusion

With some attention to detail the VDRM family of MagI³C Power Modules make excellent inverting buck-boost regulators. They offer a compact, low-EMI solution that can deliver negative output voltage for a variety of applications with a minimum of design headaches.

APPLICATION NOTE

Designing an Inverting Buck-boost Converter with MagI³C Power Module WPMDH1302401 / 171032401

(6 - 42 V_{IN} / 3A / 5 - 24 V_{OUT})

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Application Notes:
http://www.we-online.com/app-notes

REDEXPERT Design Tool:
http://www.we-online.com/redexpert

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